

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U.S. Patent Application of)
WATANABE *et al.*)
Application Number: To be assigned)
Filed: Concurrently herewith)
For: SIGNAL PROCESSING CIRCUIT)

Honorable Assistant Commissioner
for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Applicants have amended the claims in order to remove the multiple dependencies contained therein in accordance with standard U.S. practice, thereby reducing the basic filing fee.

No new matter has been added to the application as a result of this amendment. Prior to an examination on the merits, please amend the above-identified application as follows:

IN THE CLAIMS:

Please substitute claims 3-10 currently on file with the following amended claims.

3. (Amended) A signal processing circuit according to Claim 1, further comprising a second input-output circuit that is connected to said system bus, produces an interrupt request to be issued to said microprocessor, and transfers data over said system bus under control of said microprocessor.
4. (Amended) A signal processing circuit according to Claim 1, further comprising a third input-output circuit that receives or transmits a serial signal, produces an interrupt request to be issued to said microprocessor, and transfers the serial signal over said system bus under control of said microprocessor.

5. (Amended) A signal processing circuit according to Claim 1, further comprising a timer that cyclically applies an interrupt signal to said microprocessor, and a control means that includes a status register which indicates the processing state of said dedicated processing circuit, and an instruction register in which said microprocessor sets processing to be performed by said dedicated processing circuit, wherein:

said microprocessor reads a value from said status register in response to the cyclic interrupt signal, and judges whether the next processing instruction can be issued to said dedicated processing circuit; and

when the next processing instruction can be issued, said control means allows the instruction to be written in said instruction register.

6. (Amended) A signal processing circuit according to Claim 1, wherein data that should be processed by said dedicated processing circuit is stored in said local memory, and data stored in said local memory is read by way of said third connection circuit, said second local bus, and said input-output circuit.

7. (Amended) A signal processing circuit according to Claim 1, wherein said first input-output circuit is a video input-output circuit that receives or transmits video data, said dedicated processing circuit is a video processing circuit including at least one of an encoding circuit, a decoding circuit, a discrete cosine transform circuit, an inverse discrete cosine transform circuit, a motion estimation circuit, and a motion compensation circuit.

8. (Amended) A signal processing circuit according to Claim 7, wherein said memory access control circuit includes a control means that stores image data received in real-time in said local memory by way of said first input-output circuit, said second local bus, and said third connection circuit, and that transfers the image data stored in said local memory to said video processing circuit by way of said second connection circuit and said first local bus.

9. (Amended) A signal processing circuit according to Claim 7, further comprising a second input-output circuit that receives or transmits a voice signal, is connected to said system bus, produces an interrupt request to be issued to said microprocessor, and transfers data over said system bus under control of said microprocessor.
10. (Amended) A signal processing circuit according to Claim 7, further comprising a third input-output circuit that receives or transmits a serial signal that is either an encoded video signal or an encoded voice signal, produces an interrupt request to be issued to said microprocessor, and transfers data of the serial signal over said system bus under control of said microprocessor.

Please add the following new claims:

11. (Added) A signal processing circuit according to Claim 2, further comprising a second input-output circuit that is connected to said system bus, produces an interrupt request to be issued to said microprocessor, and transfers data over said system bus under control of said microprocessor.
12. (Added) A signal processing circuit according to Claim 2, further comprising a third input-output circuit that receives or transmits a serial signal, produces an interrupt request to be issued to said microprocessor, and transfers the serial signal over said system bus under control of said microprocessor.
13. (Added) A signal processing circuit according to Claim 3, further comprising a third input-output circuit that receives or transmits a serial signal, produces an interrupt request to be issued to said microprocessor, and transfers the serial signal over said system bus under control of said microprocessor.
14. (Added) A signal processing circuit according to Claim 11, further comprising a third input-output circuit that receives or transmits a serial signal, produces an interrupt request

to be issued to said microprocessor, and transfers the serial signal over said system bus under control of said microprocessor.

15. (Added) A signal processing circuit according to Claim 2, further comprising a timer that cyclically applies an interrupt signal to said microprocessor, and a control means that includes a status register which indicates the processing state of said dedicated processing circuit, and an instruction register in which said microprocessor sets processing to be performed by said dedicated processing circuit, wherein:

said microprocessor reads a value from said status register in response to the cyclic interrupt signal, and judges whether the next processing instruction can be issued to said dedicated processing circuit; and

when the next processing instruction can be issued, said control means allows the instruction to be written in said instruction register.

16. (Added) A signal processing circuit according to Claim 3, further comprising a timer that cyclically applies an interrupt signal to said microprocessor, and a control means that includes a status register which indicates the processing state of said dedicated processing circuit, and an instruction register in which said microprocessor sets processing to be performed by said dedicated processing circuit, wherein:

said microprocessor reads a value from said status register in response to the cyclic interrupt signal, and judges whether the next processing instruction can be issued to said dedicated processing circuit; and

when the next processing instruction can be issued, said control means allows the instruction to be written in said instruction register.

17. (Added) A signal processing circuit according to Claim 11, further comprising a timer that cyclically applies an interrupt signal to said microprocessor, and a control means that includes a status register which indicates the processing state of said dedicated processing circuit, and an instruction register in which said microprocessor sets processing to be performed by said dedicated processing circuit, wherein:

said microprocessor reads a value from said status register in response to the cyclic interrupt signal, and judges whether the next processing instruction can be issued to said dedicated processing circuit; and

when the next processing instruction can be issued, said control means allows the instruction to be written in said instruction register.

18. (Added) A signal processing circuit according to Claim 2, wherein data that should be processed by said dedicated processing circuit is stored in said local memory, and data stored in said local memory is read by way of said third connection circuit, said second local bus, and said input-output circuit.
19. (Added) A signal processing circuit according to Claim 3, wherein data that should be processed by said dedicated processing circuit is stored in said local memory, and data stored in said local memory is read by way of said third connection circuit, said second local bus, and said input-output circuit.
20. (Added) A signal processing circuit according to Claim 11, wherein data that should be processed by said dedicated processing circuit is stored in said local memory, and data stored in said local memory is read by way of said third connection circuit, said second local bus, and said input-output circuit.
21. (Added) A signal processing circuit according to Claim 2, wherein said first input-output circuit is a video input-output circuit that receives or transmits video data, said dedicated processing circuit is a video processing circuit including at least one of an encoding circuit, a decoding circuit, a discrete cosine transform circuit, an inverse discrete cosine transform circuit, a motion estimation circuit, and a motion compensation circuit.
22. (Added) A signal processing circuit according to Claim 21, wherein said memory access control circuit includes a control means that stores image data received in real-time in said local memory by way of said first input-output circuit, said second local bus, and

said third connection circuit, and that transfers the image data stored in said local memory to said video processing circuit by way of said second connection circuit and said first local bus.

23. (Added) A signal processing circuit according to Claim 21, further comprising a second input-output circuit that receives or transmits a voice signal, is connected to said system bus, produces an interrupt request to be issued to said microprocessor, and transfers data over said system bus under control of said microprocessor.
24. (Added) A signal processing circuit according to Claim 8, further comprising a second input-output circuit that receives or transmits a voice signal, is connected to said system bus, produces an interrupt request to be issued to said microprocessor, and transfers data over said system bus under control of said microprocessor.
25. (Added) A signal processing circuit according to Claim 22, further comprising a second input-output circuit that receives or transmits a voice signal, is connected to said system bus, produces an interrupt request to be issued to said microprocessor, and transfers data over said system bus under control of said microprocessor.
26. (Added) A signal processing circuit according to Claim 21, further comprising a third input-output circuit that receives or transmits a serial signal that is either an encoded video signal or an encoded voice signal, produces an interrupt request to be issued to said microprocessor, and transfers data of the serial signal over said system bus under control of said microprocessor.
27. (Added) A signal processing circuit according to Claim 8, further comprising a third input-output circuit that receives or transmits a serial signal that is either an encoded video signal or an encoded voice signal, produces an interrupt request to be issued to said microprocessor, and transfers data of the serial signal over said system bus under control of said microprocessor.

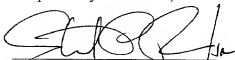
28. (Added) A signal processing circuit according to Claim 22, further comprising a third input-output circuit that receives or transmits a serial signal that is either an encoded video signal or an encoded voice signal, produces an interrupt request to be issued to said microprocessor, and transfers data of the serial signal over said system bus under control of said microprocessor.

REMARKS

Applicant has amended claim 3 and added claim 11, amended claim 4 and added claims 12, 13 and 14, amended claim 5 and added claims 15, 16 and 17, amended claim 6 and added claims 18, 19 and 20, amended claim 7 and added claim 21, amended claim 8 and added claim 22, amended claim 9 and added claims 23, 24, and 25, and amended claim 10 and added claims 26, 27 and 28. Applicants have amended the claims in order to remove the multiple dependencies contained therein in accordance with standard U.S. practice, thereby reducing the basic filing fee. No new matter has been added to the application as a result of this amendment.

In view of the above amendments and Applicants' comments stated herein, Applicants respectfully request an early and favorable action on the merits.

Respectfully submitted,



Stanley P. Fisher

Registration Number 24,344

REED SMITH HAZEL & THOMAS LLP

3110 Fairview Park Drive

Suite 1400

Falls Church, Virginia 22042

(703) 641-4200

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JUAN CARLOS A. MARQUEZ
REGISTRATION NO. 24,012

CLAIMS

1. A signal processing circuit having a data input-output circuit, a microprocessor, a dedicated processing circuit, a local memory, and a memory access control circuit interconnected over a bus, wherein:

said bus includes a system bus that is connected to said data input-output circuit, said microprocessor, said dedicated processing circuit, and said memory access control circuit, and a local memory bus that is connected to said local memory;

first, second, and third connection circuits are connected between said system bus and said local memory bus, between a first local bus included in said dedicated processing circuit and said local memory bus, and between a second local bus included in said data input-output circuit and said local memory bus; and

said memory access control circuit controls the connections of said first, second, and third connection circuits.

2. A signal processing circuit according to Claim 1, wherein said memory access control circuit controls the connections of said first, second, and third connection circuits according to the priorities predetermined for the connections.

3. A signal processing circuit according to Claim 1 ~~or 2~~, further comprising a second input-output circuit that is connected to said system bus, produces

an interrupt request to be issued to said microprocessor, and transfers data over said system bus under control of said microprocessor.

4. A signal processing circuit according to ~~any~~
5 ~~of Claims 1 to 3~~, further comprising a third input-
output circuit that receives or transmits a serial
signal, produces an interrupt request to be issued to
said microprocessor, and transfers the serial signal
over said system bus under control of said
10 microprocessor.

5. A signal processing circuit according to ~~any~~
15 ~~of Claims 1 to 3~~, further comprising a timer that
cyclically applies an interrupt signal to said
microprocessor, and a control means that includes a
status register which indicates the processing state of
said dedicated processing circuit, and an instruction
register in which said microprocessor sets processing
to be performed by said dedicated processing circuit,
wherein:

20 said microprocessor reads a value from said
status register in response to the cyclic interrupt
signal, and judges whether the next processing
instruction can be issued to said dedicated processing
circuit; and

25 when the next processing instruction can be
issued, said control means allows the instruction to be
written in said instruction register.

6. A signal processing circuit according to ~~any~~

of Claims 1 ~~to~~ 3, wherein data that should be processed by said dedicated processing circuit is stored in said local memory, and data stored in said local memory is read by way of said third connection circuit, said second local bus, and said input-output circuit.

7. A signal processing circuit according to Claim 1 ~~or~~ 2, wherein said first input-output circuit is a video input-output circuit that receives or transmits video data, said dedicated processing circuit is a video processing circuit including at least one of an encoding circuit, a decoding circuit, a discrete cosine transform circuit, an inverse discrete cosine transform circuit, a motion estimation circuit, and a motion compensation circuit.

8. A signal processing circuit according to Claim 7, wherein said memory access control circuit includes a control means that stores image data received in real-time in said local memory by way of said first input-output circuit, said second local bus, and said third connection circuit, and that transfers the image data stored in said local memory to said video processing circuit by way of said second connection circuit and said first local bus.

9. A signal processing circuit according to Claim 7 ~~or~~ 8, further comprising a second input-output circuit that receives or transmits a voice signal, is connected to said system bus, produces an interrupt request to be issued to said microprocessor, and

transfers data over said system bus under control of said microprocessor.

10. A signal processing circuit according to Claim 7 ~~or 8~~, further comprising a third input-output
5 circuit that receives or transmits a serial signal that is either an encoded video signal or an encoded voice signal, produces an interrupt request to be issued to said microprocessor, and transfers data of the serial
10 signal over said system bus under control of said microprocessor.